CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters PATENT is:

1. A method of forming a poly-poly capacitor, a MOS transistor, and a bipolar transistor simultaneously on a substrate comprising the steps of:

depositing and patterning a first layer of polysilicon on the substrate to form a first plate electrode of said capacitor and on an electrode of the MOS transistor; and

depositing and patterning a second layer of polysilicon on the substrate to form a second plate electrode of said capacitor and an electrode of the bipolar transistor,

said second layer of polsilicon comprising SiGe polysilicon.

2. The method of Claim 1 wherein electrode of the MOS transistor comprises a polysilicon gate formed on a gate oxide, said gate oxide being formed on a surface of the substrate, the substrate having source and drain regions beneath said polysilicon gate.

3. The method of Claim 2 wherein the substrate is a semiconducting material selected from the group consisting of Si, Ge, SiGe, GaAs, InAs and layered semiconductor substrates.

4. The method of Claim 2 wherein the substrate further comprises shallow trench isolation regions and a subcollector region, said subcollector region being formed between said shallow trench isolation regions.

5. A method of forming a poly-poly capacitor comprising the steps of:

(a) forming a film stack on a surface of a semiconductor structure, said structure comprising at least a gate region of a metal oxide semiconductor device and a bottom polysilicon plate of a poly-poly capacitor formed on a surface thereof, said film stack including at least a polysilicon layer;

(b) forming a bipolar opening in said film stack exposing at least a portion of said surface of said semiconductor structure, wherein said bipolar opening is formed in a region in which a bipolar device will be subsequently fabricated;

(c) simultaneously forming a SiGe epi layer in said bipolar opening, while forming a SiGe polysilicon film on exposed portions of said polysilicon layer of said film stack;

(d) selectively doping portions of said SiGe polysilicon film as well as said SiGe epi layer with a dopant atom of a first conductivity type;

(e) forming a patterned passivating layer on a portion of said doped SiGe epi layer;

(f) forming a patterned doped emitter polysilicon layer on said patterned passivating layer as well as on said doped SiGe epi layer formed in said bipolar opening thereby completing fabrication of said bipolar device, said doped emitter polysilicon layer having a different conductivity than said doped SiGe epi layer; and

(g) removing selective portions of said doped SiGe polysilicon film and remaining layers of said film stack so as to expose said gate of said metal oxide semiconductor while protecting said bipolar device region and said doped SiGe polysilicon layer overlying said bottom polysilicon plate of said poly-poly capacitor.

6. The method of Claim 5 wherein said film stack further comprises a bottom insulator layer and an optional top insulator layer.

7. The method of Claim 6 wherein said top and bottom insulator layers of said film stack are the same or different insulative materials selected from the group consisting of SiO_2 and Si oxynitrides.

8. The method of Claim 7 wherein said top and bottom insulator layers are both composed of SiO_2.

9. The method of Claim 6 wherein said top insulator layer has a thickness of from about 100 to about 1000 Å.

10. The method of Claim 6 wherein said bottom insulator layer has a thickness of from about 50 to about 1000 Å.

11. The method of Claim 5 wherein said polysilicon layer has a thickness of from about 100 to about 1000 Å.

12. The method of Claim 5 wherein said bipolar opening is formed by employing lithography and etching.

13. The method of Claim 12 wherein said etching is carried out by reactive-ion etching or ion beam etching.

14. The method of Claim 6 wherein said optional top insulator layer is removed utilizing an etch process that is highly selective in removing said top insulator layer as compared to said underlying polysilicon layer.

15. The method of Claim 5 wherein said SiGe epi layer and said SiGe polysilicon film are formed simultaneously utilizing a deposition process that is carried out at temperatures of from about 900°C or below.

16. The method of Claim 15 wherein said temperature of said deposition process is from about 400° to about 500°C.

17. The method of Claim 5 wherein said SiGe epi layer and said SiGe polysilicon film have the same or different thickness.

18. The method of Claim 17 wherein said SiGe epi layer and said SiGe polysilicon film have the same thickness, said thickness of each layer being of from about 1000 to about 5000 Å.

19. The method of Claim 5 wherein said dopant used in doping said SiGe epi layer is boron having a concentration of about $4x10^{15}$ atoms/cm^2.

20. The method of Claim 5 wherein said dopant used in doping said emitter polysilicon is As.

21. The method of Claim 5 wherein said patterned emitter doped polysilicon layer is formed by depositing a layer of polysilicon, doping said layer with a dopant and thereafter subjecting said emitter doped polysilicon layer to lithography and etching.

22. The method of Claim 1 wherein optional spacers are formed on said poly-poly capacitor.

23. The method of Claim 22 wherein said optional spacers are formed by deposition, lithography and etching.

sub a2

24. A poly-poly capacitor comprising two plate electrodes, wherein at least one of said plate electrodes is composed of SiGe polysilicon, said plate electrodes being separated by an insulator structure.

25. The poly-poly capacitor of Claim 24 wherein one of said plate electrodes is composed of polysilicon and the other plate electrode is composed of SiGe polysilicon.

26. The poly-poly capacitor of Claim 24 wherein both of said plate electrodes are composed of SiGe polysilicon.

27. The poly-poly capacitor of Claim 24 wherein at least one said plate electrodes is polysilicon from a FET gate or a bipolar emitter.

28. The poly-poly capacitor of Claim 24 further including a bipolar device region and a FET region, wherein said capacitor, bipolar device region and FET region are electrically isolated from each by isolation regions.

29. A semiconductor device, comprising

a capacitor having first and second plate electrodes, one of said plate electrodes being comprised of a first conductive patterned layer; and

a bipolar device having first and second electrodes, one of said electrodes being comprised of said first conductive patterned layer;

wherein said first conductive patterned layer is comprised of SiGe material.

30. A semiconductor structure, comprising

a first layer of polysilicon patterned to form a first electrode of a MOS device and a first plate electrode of a capacitor, and

a second layer of SiGe polysilicon patterned to form a first electrode of a bipolar device and a second plate electrode of said capacitor,

said second layer being comprised of SiGe polysilicon.